



IPW

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Teck Kheng Lee

Serial No.: 10/829,647

Filed: April 22, 2004

For: METHODS FOR ASSEMBLY AND
PACKAGING OF FLIP CHIP
CONFIGURED DICE WITH INTERPOSER

Confirmation No.: 6967

Examiner: Unknown

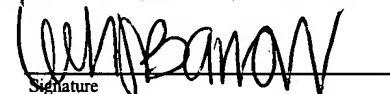
Group Art Unit: 2812

Attorney Docket No.: 2269-4974.1US
(00-0693.01/US)

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Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 or PTO/SB/08 be considered by the Examiner and made of record. Copies of U.S. patents are not being submitted pursuant to M.P.E.P. 609 III A(2). Copies of foreign patent documents and non-patent literature are enclosed pursuant to 37 C.F.R. § 1.98(a)(2).

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicants herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

U.S. Patent Documents

<u>U.S. Patent No.</u>	<u>Publication Date</u>	<u>Patentee</u>
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US - 6,291,265	09/2001	Mess
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<u>Document No.</u>	<u>Publication Date</u>	<u>Patentee</u>
EP 684644	11/1995	Kata et al.
EP 1009027	06/2000	Okuno
KR 2001054744	07/2001	Choi et al. (English Abstract)

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AL-SARAWI et al., A review of 3-D packaging technology, @ Components, Packaging, and Manufacturing Technology, Part B: IEEE Transactions on Advanced Packaging, Vol 21, Issue 1, Feb. 1998, pp. 2-14.

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KLOESER et al., A Fine Pitch Stencil Printing of Sn/Pb and Lead Free Solders for Flip Chip Technology, @ IEEE Transactions of CPMT - Part C, vol. 21, No. 1, 1998, pp. 41-49.

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- "The 2003 International Technology Roadmap for Semiconductor: Assembly and Packaging."
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- XIAO et al., "Reliability study and failure analysis of fine pitch solder-bumped flip chip on low-cost flexible substrate without using stiffener," IEEE, 2002. Proceedings 52nd, 28-31 May 2002, pp. 112-118.

Applicants offer to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

Serial No. 10/829,647

This Supplemental Information Disclosure Statement is filed before the mailing date of a first Office Action on the merits.

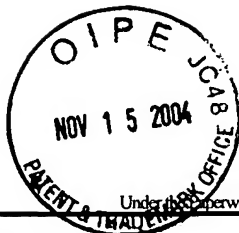
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Date: November 12, 2004
TNB/lmh:ljb

Enclosures: Form PTO-1449 or PTO/SB/08
Copy of non-US documents cited

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PTO/SB/08A (10-01)

Approved for use through 10/31/2002. OMB 0651-0031

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet 1 of 4

Complete if Known

Application Number	10/829,647
Filing Date	April 22, 2004
First Named Inventor	Teck Kheng Lee
Group Art Unit	2812
Examiner Name	Unknown
Attorney Docket Number	2269-4974.1US (00-0693.01/US)

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Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
		US-3,239,496	03/1966	Jursich	
		US- 4,074,342	02/1978	Honn et al.	
		US- 4,818,728	04/1989	Rai et al.	
		US- 5,148,265	09/1992	Khandros	
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		US- 6,022,761	02/2000	Gruppen-Shemansky et al.	
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		US- 6,177,723	01/2001	Eng et al.	
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		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				
		EP 684644	11/1995	Kata et al.		
		EP 1009027	06/2000	Okuno		
		KR 2001054744	07/2001	Choi et al.		x

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				Application Number	10/829,647
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				Group Art Unit	2812
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Sheet	2	of	4		

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		US - 6,756,251	06/2004	Lee	
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		US - 2002/0185661 A1	12/2002	Kawanobe et al.	
		US - 2003/0134450 A1	07/2003	Lee	

[illegible]

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Sheet

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Application Number

10/829,647

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April 22, 2004

First Named Inventor

Teck Kheng Lee

Group Art Unit

2812

Examiner Name

Unknown

Attorney Docket Number

2269-4974 IUS (00-0693 01/IUS)

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
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